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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/973,843	10/11/2001	Taisuke Iwai	108391-00020	7702

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EXAMINER	
SHINGLETON, MICHAEL B	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/973,843	IWAI, TAISUKE	
	Examiner	Art Unit	
	Michael B. Shingleton	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *4,6-8,10 and 12-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,27 and 28* is/are rejected.

7)☒ Claim(s) *3,5,9 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's election without traverse of Species II directed toward Figures 3 and 4 in the reply filed on June 23, 2004 is acknowledged.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iyer et al. 6,130,579 (Iyer) in view of Segal 4,555,672 (Segal).

Figure 1 of Iyer discloses an amplifier having a front amplification stage 102 and a rear amplification stage 104. As is clearly illustrated the rear stage 104 amplifies the output from the front stage and is "disposed immediately after said front amplification stage" (Note that no inter-stage matching circuit is disposed in between.). Claim 1 recites "wherein amplification unit that forms a part of the plurality of amplification unit perform on/off switching of amplification operation according to an RF input of the front amplification stage or increase a bias current as the RF input increases". Iyer clearly has the second item of this alternative expression. Namely, "the amplification unit...perform...increase a bias current as the RF input increases" and thereby meets this limitation (Note column 3, around line 35 of Iyer). Iyer is silent on the details of the front and rear amplification stages. Iyer is silent on the rear stage being composed of "a plurality of amplification unit connected in parallel".

Segal discloses that it well known to utilize "a plurality of amplification unit connected in parallel" for one power amplifier unit. Note Figure 1.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to have utilized a power amplifier that is composed of a plurality of amplification units connected in parallel because, as the Iyer reference is silent on the exact form of the amplification stages one of ordinary skill in the art would have been motivated to use any art-recognized equivalent power amplifier unit for Iyer such as the conventional plurality of amplification unit connected in parallel for the power amplifier unit as taught by Segal. One of

ordinary skill additionally would have been motivated to make the modification so as to hold down the total capacitance thereby maintaining excellent high-frequency operation as taught by Segal (See column 4, around line 32).

Claims 2, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iyer et al. 6,130,579 (Iyer) in view of Segal 4,555,672 (Segal) and Ishikawa et al. 5,982,236 (Ishikawa).

Figure 1 of Iyer discloses an amplifier having a front amplification stage 102 and a rear amplification stage 104. As is clearly illustrated the rear stage 104 amplifies the output from the front stage and is "disposed immediately after said front amplification stage". Element 14 clearly forms a rear stage DC bias control circuit that controls the bias of the rear stage. Iyer is silent on the rear stage being composed of "a plurality of amplification unit connected in parallel", the use of a inter-stage matching circuit and the use of transistors for the amplification stages.

Segal discloses that it well known to utilize "a plurality of amplification unit connected in parallel" for one power amplifier unit. See Figure 1. Segal also discloses that it is well known to use transistors to make up these units and to make up amplifiers in general.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to have utilized a power amplifier that is composed of a plurality of amplification units connected in parallel for the rear amplification stage because, as the Iyer reference is silent on the exact form of the amplification stages one of ordinary skill in the art would have been motivated to use any art-recognized equivalent power amplifier unit for Iyer such as the conventional power amplifier unit as taught by Segal. One of ordinary skill additionally would have been motivated to make the modification so as to hold down the total capacitance thereby maintaining excellent high-frequency operation as taught by Segal (See column 4, around line 32).

Also accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized transistors to make up the front and rear stage units because as the Iyer reference is silent on the exact form of the amplification stages one of ordinary skill in the art would have been motivated to use any conventional amplifying element to make the amplification units such as the conventional transistor.

The use of inter-stage matching circuit, i.e. matching circuits between amplification stages is well known in the art so as to match the impedance between stages as taught by Ishikawa (See column 2, around line 30).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided an inter-stage matching circuit between the front and rear stages of Iyer so as to match the impedance between stages as taught by Ishikawa..

Iyer is likewise silent on forming on one chip via integration the front and rear stages and the inter-stage matching circuit. It is well-known to integrate a circuit so as to make a more compact unit, and a more reliable/robust circuit.

Thus it would have been obvious to one of ordinary skill in the art to have integrated the circuit on one chip so as to form a more compact circuit and a more reliable/robust circuit as is well known in the art.

Iyer is likewise silent on providing the circuit mentioned above on two or more chips. The integration of a circuit as noted above makes for a more compact unit and more reliable/robust circuit. It is likewise well known that the use of plural chips for make up a circuit allows for the replacement of parts of the circuit while still maintaining the basic benefits of a more compact unit and a more reliable/robust circuit.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided the circuit on two or more semiconductor chips so as to allow for replacement of parts of the circuit while maintaining the basic benefits of a integrated circuit i.e. the more compact unit and more reliable/robust circuit as is well known in the art.

Claims 3, 5, 9 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Furuya et al. JP 06053761 A discloses the general state of the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571)272-1770. The examiner can normally be reached on Tues-Fri from 8:30 to 4:30. The examiner can also be reached on alternate Mondays. The examiner normally has second Mondays of the bi-week off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
August 18, 2004

MICHAEL B SHINGLETON
PRIMARY EXAMINER
GROUP ART UNIT 2817